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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,721	10/07/2003	Fabio Pellizzer	854163.408	2650

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EXAMINER	
RICHARDS, N DREW	
ART UNIT	**PAPER NUMBER**
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

CT

Office Action Summary	Application No. 10/680,721	Applicant(s) PELLIZZER ET AL.	
	Examiner N. Drew Richards	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-19 and 27-36* is/are rejected.

7)☒ Claim(s) *20-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date *3/4/04,3/25/04*.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group II, claims 12-26 in the reply filed on 12/16/04 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Newly added claims 27-36 read on the elected invention. Thus, claims 12-36 have been examined.

Claim Objections

2. Claims 12, 20, 27, 28 and 32 are objected to because of the following informalities:

- Claim 12 lines 13-14 recites "and" twice, it is suggested that one of the terms be removed;
- Claim 20 line 13 should read "**the** first conduction region" as the first conduction region has previously been recited in line 3; line 14 should read "the **first** conduction region" so as to properly claim applicants invention; line 15 should read "**a** first region" as a first region has not previously been recited; line 17 should read "the **first** conduction region" so as to properly claim applicants invention; line 18 should read "the **first** conduction region" so as to properly claim applicants invention;
- Claim 27 line 6 recites "forming **a** control regions" where it should recite "forming control regions", line 13 should recite "a plurality **of** second";

- Claim 28 line 2 should recite "the second conduct**ion** regions" to properly employ the same terminology previously used in claim 27;
- Claim 32 line 2, "regions" should be "region" to properly claim a singular region.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 27-31, 33, 34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakata et al. (U.S. Patent No. 6,573,586 B2) in view of Tanomura (U.S. Patent No. 6,403,436 B1).

With regard to claim 27, Sakata et al. teach a memory cell array (array shown in figures 9, 12, 14 and 19) comprising:

- a plurality of storage elements (figure 10; 110/111/112/113 define the storage elements); and
- a plurality of selection transistors including:
    - a plurality of active area regions 103 of a second conductivity type and a first doping level forming control regions of the selection transistors (figure 10; 103 is the base region which is a control region formed of second conductivity type P-type at a first (unspecified) doping level);

- a plurality of first conduction regions 104 of the first conductivity type formed in the active area regions 103 and respectively forming first conducting regions of the selection transistors (figure 10; 104 is the emitter region which is a first conduction region of first conductivity type N-type);
- a plurality of control contact regions 105 of the second conductivity type and a second doping level, higher than the first doping level, formed in the active area regions 103 (figure 10; 105 is the lead-out portion of the base; though the relative doping level of region 105 compared to region 103 is not explicitly disclosed, it is nonetheless obvious to one of ordinary skill in the art that region 105 will have a higher dopant concentration; first it is obvious since region 105 is doped twice while region 103 is only doped once, region 105 is doped in the step to dope region 103 since the ion implantation for region 103 is carried out everywhere not surrounded by pattern IIC of figure 9 (column 5 lines 14-19) and then doped a second time in accordance with pattern IIB (column 5 lines 20-28), thus region 105 necessarily contains the total dopant concentration of the two separate doping steps; second even if the reference is not considered to positively teach 105 having a higher dopant concentration, it would have been obvious to one of ordinary skill in the art at the time of the invention to form region 105 with a higher dopant concentration so that a lower resistance and better ohmic contact can be made to the region); and

- a plurality of second conduction region 101n of the selection transistors, the second conduction regions 101n being respectively coupled to the active regions 103 (figure 10).

Sakata et al. do not teach a semiconductor body of the first conductivity type where the active regions (base regions) overlie the semiconductor body. Sakata et al. teach a bipolar transistor including a collector region 101n, a base region 103, and an emitter region 104, but do not teach the semiconductor body underneath.

Tanomura teaches a bipolar transistor in figure 1, for example. Tanomura teach a subcollector region 105/106, a collector layer 104 overlying the subcollector region, a base layer 103 overlying the collector and subcollector region, and an emitter layer 102 overlying the base region, collector region, and subcollector region. The subcollector region 105/106 corresponds to the semiconductor body of a first conductivity type as claimed, the collector layer 104 corresponds to the second conduction region claimed, the base region 103 corresponds to the active region claimed, and the emitter layer 102 corresponds to the first conducting regions claimed. The bipolar transistor of Tanomura is similar to that of Sakata et al. in that it is a vertical bipolar transistor with the emitter formed over the base and collector.

Sakata et al. and Tanomura are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include a subcollector (semiconductor body of first conductivity type) under the base layer and collector layer. The motivation for doing so is to provide a subcollector layer to reduce collector resistance (Tanomura column 3 lines 62-67).

Therefore, it would have been obvious to combine Sakata et al. with Tanomura to obtain the invention of claim 27.

With regard to claim 28, Sakata et al. teach that the second conduction regions 101n are collector regions (column 5 lines 4-5), the first conduction regions 104 are emitter regions (column 5 lines 20-22), and the active areas 103 are base regions (column 5 lines 14-15). Sakata et al. show in the specific embodiment of figure 10, that the transistor is an NPN transistor. However, on column 12 lines 41-60 Sakata et al. teach that the transistor in the memory cell can alternatively be a PNP bipolar transistor structure. Thus, Sakata et al. is considered to teach the selection transistor being a PNP transistor.

With regard to claim 29, as seen in figure 11 of Sakata et al. (perpendicular cross section to that shown in figure 10), the second conduction regions 101n are contiguous with one another and form a common conduction region 101n.

With regard to claim 30, the semiconductor body (subcollector) of Tanomura includes a substrate 106 extending below the second conduction regions 104 and having a first conductivity type and an intervening conduction region 105 extending between the substrate 106 and the second conduction region 104, the intervening conduction region also having the first conductivity type. In combination with Sakata, the semiconductor body extends beneath common conduction regions as explained with regard to claim 29 above. Though not explicitly stated, it is nonetheless obvious to one of ordinary skill in the art that the intervening conduction region 105 (subcollector) will have a doping level higher than the second conduction region. Tanomura teaches the subcollector decreasing the resistance of the bipolar transistor. One of ordinary skill in the art would recognize that the subcollector would be formed with a higher dopant level in order to create a lower resistance layer. It is known in the semiconductor art that a higher dopant level is used to reduce the resistance of a semiconductor material.

With regard to claim 31, the storage components are phase change memory elements. Sakata et al. teach the storage components being ferromagnetic tunnel junction elements. These are considered "phase change" elements as the phase (direction of magnetization) is changed from to produce high or low resistance. It is noted that the claim language does not require the "phase change" to signify any particular type of phase change, thus a magnetic phase change reads on the claim as written.

With regard to claim 33, Sakata et al. teach an alternate layout in figure 13. This layout has the same basic structure as that of figure 10, but it teaches the first conduction regions 204 (analogous to region 104 of figure 10) include a plurality of pairs of first conduction regions 204 that are each positioned between two consecutive regions of the control contact regions 205 (analogous to region 105 of figure 10). Figure 13 shows one cell of the array where regions 204 are formed on the outside (in the figure, towards the edges of the figure) of regions 205. However, when considering the array of cells shown in figure 13 by placing a second and third identical cell on the left and right sides of the cell shown, pairs of regions 204 are between two consecutive regions 205, thus reading on the invention of this claim.

With regard to claim 34, Sakata et al. further teach a plurality of insulating regions 202 between the first conduction regions 204 of each pair of fist conduction regions.

With regard to claim 36, Sakata et al. further teach a plurality of conductive biasing lines 108 each connected to a plurality of the first conduction regions 104 (figure 10, column 5 lines 31-37).

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 12-19 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of copending Application No. 10/680727 in view of Gill et al. (U.S. Patent No. 6,531,373). Although the conflicting claims are not identical, they are not patentably distinct from each other because the differences between the claims of the instant invention and the copending claims would have been obvious to one of ordinary skill in the art at the time of the invention.

For example, claim 12 of the instant application is obvious over claim 1 of the copending application since claim 1 of the copending application recites all the limitations of claim 12 except for the control contact regions being connected to biasing lines. Nonetheless, connecting the control contact regions to biasing lines is considered obvious to one of ordinary skill in the art at the time of the invention. One of ordinary skill in the art would connect a biasing line in order to operate the claimed bipolar transistor and to allow reading and writing of data in the claimed memory array. If no connection was made to the control contact region (and thus the active region), then the claimed bipolar transistor and memory array would not be functional in its read and write operations. Gill et al. teach that it is known to connect a biasing line (WL) to a base region of a bipolar transistor in a phase change memory array as see in figure 1. It is noted that the base region of Gill et al. corresponds to the active region and control contact region of the copending application claim 1. Gill provides evidence that it was known in the art at the time of the invention to connect a biasing line as claimed in forming an operable memory array.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

7. Claims 27-36 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 20-26 of copending Application No. 10/680727 in view of Tanomura (U.S. Patent No. 6,403,436 B1). Although the conflicting claims are not identical, they are not patentably distinct from each other because the differences between the claims of the instant invention and the copending claims would have been obvious to one of ordinary skill in the art at the time of the invention.

For example, claim 27 of the instant application is obvious over claim 20 of the copending application since claim 20 of the copending application recites all the limitations of claim 27 except for the semiconductor body of a first conductivity type. It is noted that the active area regions of the copending application claim 20 form control regions even though the claim does not explicitly state such. Tanomura teaches in figure 1 a bipolar transistor that includes a semiconductor body region 105/106 with active areas 103, first conduction regions 102, and second conduction regions 104 formed above the semiconductor body.

Copending claim 27 and Tanomura are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include a subcollector (semiconductor body of first conductivity type) under the base layer and collector layer. The motivation for doing so is to provide a subcollector layer to reduce collector resistance (Tanomura column 3 lines 62-67). Therefore, it would have been obvious to combine copending claim 27 with Tanomura to obtain the invention of claim 27.

As further example, with regard to claim 28, the semiconductor body of Tanomura includes a substrate 106 of the first conductivity type and an intervening conduction region 105 extending between the substrate 106 and the conduction region 104. Though not explicitly stated, it is nonetheless obvious to one of ordinary skill in the art that the intervening conduction region 105 (subcollector) will have a doping level higher than the second conduction region. Tanomura teaches the subcollector decreasing the resistance of the bipolar transistor. One of ordinary skill in the art would recognize that the subcollector would be formed with a higher dopant level in order to create a lower resistance layer. It is known in the semiconductor art that a higher dopant level is used to reduce the resistance of a semiconductor material.

This is a provisional obviousness-type double patenting rejection.

Allowable Subject Matter

8. Claims 20-26 would be allowable if rewritten or amended to overcome the objection(s), set forth in this Office action.

9. The following is a statement of reasons for the indication of allowable subject matter: Prior art of record fails to teach, disclose or suggest, either alone or in combination, the memory device including the combination of limitations recited in claim 20. More specifically, prior art does not teach the first conduction region of the first conductivity type formed in, and surrounded by, the active region and the first conduction region being spaced apart laterally from the base contact region by a first portion of the active region.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Dennison (U.S. Patent No. 6,649,928 B2), Reinberg (U.S. Patent No. 5,789,758), Forbes (US 2004/0041236 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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